An HBr/Ar atomic layer etch process for precision gate recess etching of GaN-based transistors

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1. Introduction

Atomic layer etch (ALE), a technique of controllably removing layers of material with sub-nanometre precision by using sequential self-limiting reactions, has been studied for almost 30 years [1,2]. In this work, we report an HBr chemistry based ALE process to etch III-nitrides. This process induces little degradation to the electrical transport properties of GaN-based transistor material structures making it highly suitable for gate recess etching of GaN-based transistors where nanometric etch depth control is required for threshold voltage uniformity.

2. Experiment and Results

This investigation was undertaken in an Oxford Instrument PlasmaLab Inductively Coupled Plasma (ICP) etching system with repeat loop function. The HBr/Ar etch chemistry and process conditions were selected to enable the self-limited formation of Group 3(Al, Ga or In)-bromides on the semiconductor surface as a consequence of exposure to the HBr. These Group 3-bromides can then be selectively removed by a low power Ar plasma. The energy of the Ar ions is sufficient to remove the Group 3-bromides surface layer, but not the underlying, unmodified Group 3-nitride materials.

Fig.1 shows schematics of device structures which would benefit from this approach. Fig. 1(a) is a normally off, enhancement-mode (e-mode) “dual barrier” device [3], and Fig. 1(b) is an e-mode ”single barrier” transistor. In both device structures, the transistor threshold voltage is determined by the depth of the recess into which the gate is ultimately placed. The structures of Fig. 1 were grown by MOCVD on a 6” silicon substrate, and subsequently patterned by photolithography using Shipley S1818 to define the etch mask.

The ALE process has been optimised by varying a number of conditions including degree of surface ”bromidisation” by either flowing HBr gas across the wafer, or by striking a plasma; diluting the HBr in Ar by different amounts; changing the gas flow rate; and modifying the chamber pressure. In addition, the Ar plasma etch parameters including RF power; chamber pressure; and etch time were varied. The etched surface morphology, etch depth and etch trench sidewall profile were characterised by AFM and SEM. Fig. 2 shows the results of this metrology on a sample which was etched for 160 cycles using the optimised process conditions stated in the caption of Fig. 2. Surface RMS roughness of 0.9 nm (identical to that before etching) in an area of 10x10 μm was observed. Based on Van der Pauw evaluation, flowing HBr gas across the sample surface did not result in any change in sheet resistance, electron mobility or channel electron concentration. The impact of Ar plasma RF power on the electrical transport properties of the single barrier AlGaN/GaN structure (Fig 1(b)) is shown in Fig. 3 – the other process parameters are in the caption of Fig. 2. This demonstrates that low damage etching can be achieved for Ar plasma powers of less than 25 W with an etch rate of 0.13 nm/cycle.

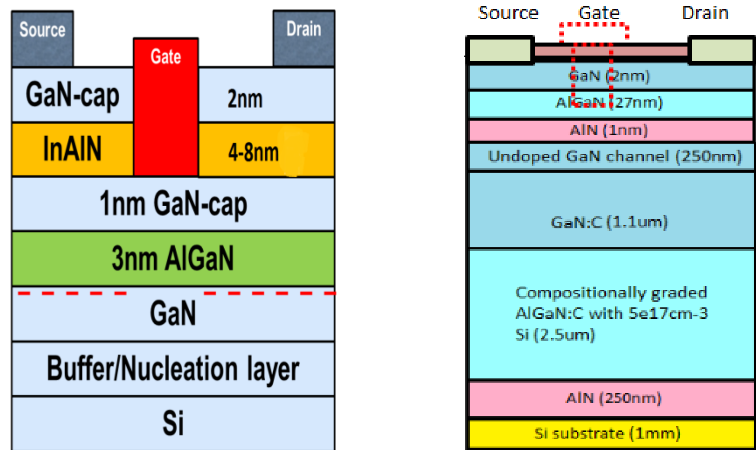

Fig 1(a): Gate recessed dual barrier e-mode device Fig 1(b): Gate recessed single barrier e-mode device

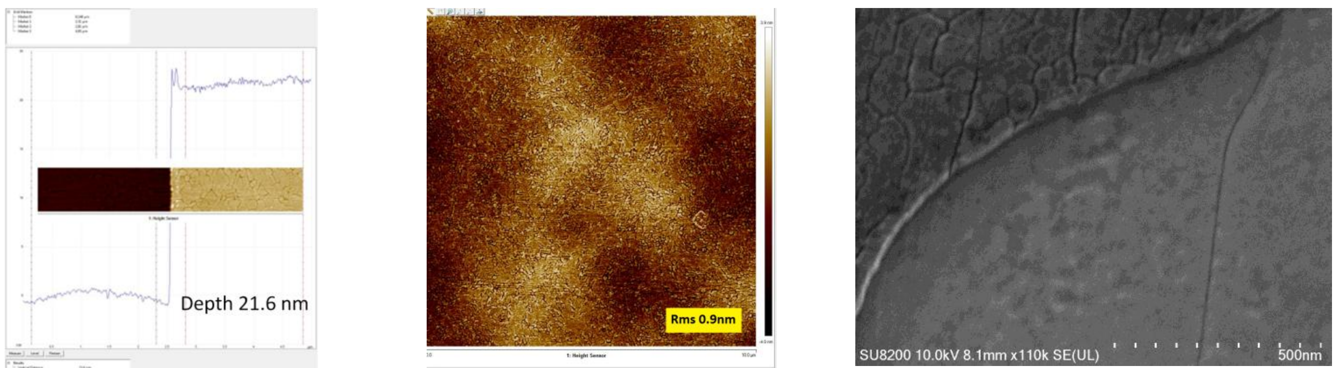

Fig.2 Etching depth by AFM (left); roughness of etching area (scan range 10x10 μm) by AFM (same as that before etching) (middle); SEM image of the etched step (right) (etch conditions : 160 cycles of : surface modification step - HBr:Ar = 7sccm:42sccm for 2 seconds without plasma, modified layer removal step – Ar = 50sccm, 20W RF power for 10secs, 50mTorr pressure at 20°C) An etch rate of 0.13 nm/cycle was achieved.

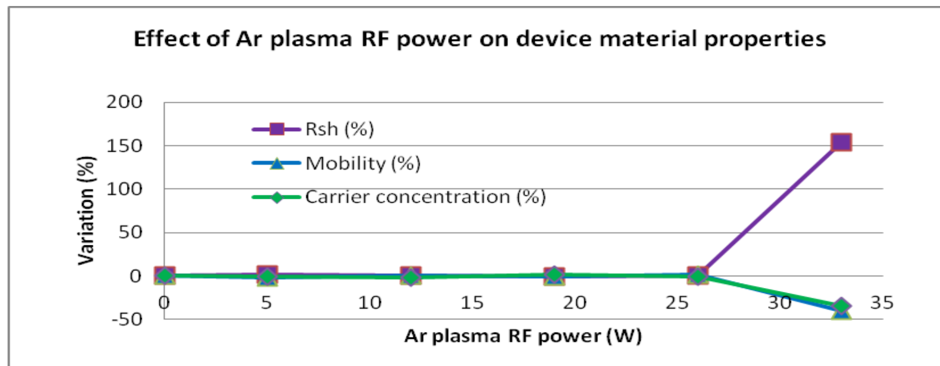

Fig.3 Effect of Ar plasma RF power on sheet resistance, carrier mobility and concentration of the d-mode AlGaN/GaN device materials after exposing Van der Pauw devices on the samples directly to Ar plasma for 60secs

Acknowledgments

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References

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