# Electrical characterisation of InAlN/AlGaN/GaN HEMT on Si substrate with varying InAlN thickness

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## Introduction

Semiconductor nitrides such as aluminium nitride (AIN), gallium nitride (GaN) and indium nitride (InN) are attractive for high power applications due to their large band gap, high critical electric field and good electron transport properties. These materials and their ternary alloys, especially AlGaN and GaN are widely used in high electron mobility transistors, where 2-D electron gas (2DEG) sheet charge is created by spontaneous and piezoelectric polarisation at the AlGaN/GaN interface [1]. Compared to AlGaN/GaN, InAlN based heterostructures can induce higher quantum well polarisation charges, which in turn result in higher device currents [2].

Hiroki et al [3-4] have demonstrated the growth of InAlN/AlGaN/GaN on sapphire (Al<sub>2</sub>O<sub>3</sub>) substrates. They tested Schottky gate HEMT based on these structures and reported improved gate leakage current and sub-threshold swing compared to devices that use an InAlN/AlGaN based structure with similar barrier heights. These promising epi-layer structures are limited by the choice of substrate. An extension of the technology to silicon substrates is more costeffective and important for future commercialisation.

In this work, we have demonstrated InAlN/AlGaN/GaN HEMT on Si substrates and characterised three wafers with different InAlN thicknesses using room temperature Hall measurements and transfer length method (TLM) measurements.

### **Experiments and Results**

The HEMT structures were grown on 6'' diameter silicon wafer by MOCVD. The

structures were first isolated by a 600nm deep mesa etch using SiCl<sub>4</sub> reactive ion etching (RIE). Consequently, Ti/Al/Ni/Au source and drain ohmic contacts of 30/180/40/100 nm thicknesses were deposited by lift-off and annealed at  $770^{\circ}$  C for 30s in N<sub>2</sub> atmosphere. This was followed by the formation of Schottky gate Ni/Au contacts of 20/200 nm thicknesses, also using the lift-off technique.

Ti/Al/Ni /Au	Ni/Au	Ti/Al/Ni /Au			
2nm GaN					
InAIN					
1nm GaN					
3nm AlGaN					
Buffer & Nucleation layers					
Si					

Fig.1. InAlN/AlGaN/GaN HEMT layer structure.

Table 1: TLM and Hall measurements for varying InAlN thicknesses.

	Т	`LM	Hall measurements		
x nm InAlN	R <sub>c</sub> (Ωmm)	R <sub>sh</sub> (Ω/sq)	R <sub>sh</sub> (Ω/sq)	µ <sub>н</sub> (cm²/Vs)	n <sub>H</sub> (x10 <sup>13</sup> cm <sup>-2</sup> )
x = 5nm	0.95	273	277	1540	1.47
x = 6nm	0.67	300	301	1370	1.52
x = 8nm	0.67	306	323	1060	1.82



Fig.2. DC output characteristics of 8nm InAlN/3nm AlGaN/GaN HEMT ( $W_g=100\mu m$ ,  $L_{ds}=12\mu m$ ,  $L_g=3\mu m$ ).



Fig.3. Comparison of transfer characteristics for 8nm InAlN (black) and 5nm InAlN (blue). The increased polarisation-induced charge for thicker (8nm) InAlN, results in a more negative threshold voltage.  $(W_g=100\mu m, L_{ds}=12\mu m, L_g=3\mu m)$ 

The low sheet and contact resistances as well as the smooth surface of the wafers grown resulted in high maximum currents  $I_{DS} > 600 \text{mA/mm}$  and transconductance  $g_m > 200 \text{ mS/mm}$ .

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